UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,661	12/09/2003	Robert Eric Fesler	P05727 (NATI15-05727)	6371

23990 7590 05/24/2007

DOCKET CLERK
P.O. DRAWER 800889
DALLAS, TX 75380

EXAMINER	
MANOSKEY, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2113	
MAIL DATE	**DELIVERY MODE**
05/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/731,661	FESLER, ROBERT ERIC	
	Examiner	Art Unit	
	Joseph D. Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6-10, 12-15, 17-19, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Jacks et al., U.S. Patent 5,740,178, hereinafter referred to as "Jacks".

3. Referring to claim 1, Jacks teaches an EEPROM having data to be copied into the RAM, "shadow memory", and the EEPROM having hash sums that should reflect the state of the initialized RAM, this is interpreted as a system for verifying data in a shadow memory, comprising: a shadow memory initializer operable to detect an initialization event, to initialize a shadow memory based on the initialization event, and to calculate original verification data for the shadow memory; the shadow memory comprising a shadow data (column, 1, lines 35-61, column 4 lines 13-17, column 5 lines 7-23). Jacks also teaches checking the initializing process by generating CRC sums over the contents of the RAM and comparing them with pre-stored CRC sums, this is interpreted as a shadow memory verifier operable to detect a verification event and to

verify the shadow data based on the verification event by calculating current verification data for the shadow memory and determining whether the current data matches the original verification data (column 1, lines 55-58 and column 4 lines 27-41).

4. As per claim 2, Jacks discloses: The system of Claim 1, wherein the shadow memory initializer is operable to initialize the shadow memory by storing the original verification data for the shadow memory (column 5 lines 7-23).

5. As per claim 3, Jacks discloses: The system of Claim 2, wherein, the shadow data verified is when the current verification data matches the original verification data and the shadow data rejected when the current verification data fails to match the original verification data (column 4 lines 27-41).

6. As per claim 4, Jacks discloses: The system Claim 3, wherein the initialization event comprises one of: the system being powered up (column 4 lines 43-45) and the shadow data being rejected (column 4 lines 41-43).

7. As per claim 6, Jacks teaches an EEPROM, "main memory", and a RAM, "shadow memory" and wherein the EEPROM contains data to be copied into the RAM, this is interpreted as a system for verifying data in a shadow memory, comprising: a main memory operable to store main data persistently; and a shadow memory operable to store shadow data temporarily, the shadow data comprising a copy of the main data

(column 2 lines 33-41, column 1 lines 35-60). Jacks also teaches the EEPROM having hash sums that should reflect the state of the initialized RAM, this interpreted as a shadow memory initializer operable to detect an initialization event and initialize the shadow memory based on the initialization event, and to calculate original verification data for the shadow memory (column 1, lines 35-60, column 4 lines 13-17, column 5 lines 7-23).

Jacks also teaches checking the initializing process by generating CRC sums over the contents of the RAM and comparing them with pre-stored CRC sums, this is interpreted as a shadow memory verifier operable to detect a verification event and to verify the shadow data based on the verification event by calculating current verification data for the shadow memory and determining whether the current data matches the original verification data (column 1, lines 55-58 and column 4 lines 27-41).

8. As per claim 7, Jacks discloses: The system of Claim 6, wherein the shadow memory initializer is operable to initialize the shadow memory by storing the original verification data for the shadow memory (column 5 lines 7-23).

9. As per claim 8, Jacks discloses: The system of Claim 7, wherein the shadow data is verified when the current verification data matches the original verification data and the shadow data rejected when the current verification data fails to match the original verification data (column 4 lines 27-41).

10. As per claim 9, Jacks discloses: The system of Claim 8, wherein the initialization event comprises one of: the system being powered up (column 4 lines 43-45) and the shadow data being rejected (column 4 lines 41-43).

11. As per claim 10, Jacks discloses: The system of Claim 7, wherein the shadow memory initializer is operable to store the original Verification data in the shadow memory (column 5 lines 7-23).

12. As per claim 12, Jacks discloses: The system of Claim 6, wherein the main memory comprises an EEPROM and the shadow memory comprises a RAM (column 1 lines 59-61).

13. As per claim 13, Jacks teaches an EEPROM that contains data to be copied to an RAM, "shadow memory", and the EEPROM containing hash sums which should reflect the initialized state of the RAM, this is interpreted as a method for verifying data in a shadow memory, comprising: initializing a shadow memory, the shadow memory comprising shadow data; calculating original verification data for the shadow memory (column 1, lines 35-60 and column 4 lines 13-17). Jacks discloses checking the initialization process of the RAM by comparing generated CRC sums with the pre-stored CRC sums, this is interpreted as detecting a verification event and verifying the shadow data based the verification event by calculating current verification data for the shadow

memory and determining whether the current verification data matches the original verification data (column 1, lines 55-58, column 4, lines 27-41 and column 5 lines 7-23).

14. As per claim 14, Jacks discloses: The method of Claim 13, further comprising detecting an initialization event, wherein initializing the shadow memory comprises initializing the shadow memory based on the initialization event (column 5 lines 7-23).

15. As per claim 15, Jacks discloses: The method of Claim 13, wherein initializing the shadow memory comprises copying main data stored a main memory into the shadow memory, and storing the original verification data (column 4 lines 13-17).

16. As per claim 17, Jacks discloses: The method Claim 13, further comprising verifying the shadow data as valid when the current verification data matches the original verification data (column 4 lines 27-41).

17. As per claim 18, Jacks discloses: The method of Claim 13, further comprising rejecting the shadow data when the current verification data fails to match the original verification data (column 4 lines 27-41).

18. As per claim 19, Jacks discloses: The method of Claim 18, wherein the initialization event comprises one of: a system being powered up (column 4 lines 43-45) and the shadow data being rejected (column 4 lines 41-43).

19. Referring to claim 21, Jacks teaches the EEPROM is copied to various parts of the RAM, and to insure memory has been properly copied a series of CRC sums are generated, this is interpreted as wherein verifying the shadow data comprises calculating the current verification data using one or more random entries within the shadow memory (column 1, lines 49-58).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 5, 11, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacks in view of Meyer, U.S. Patent 5,953,352.

22. As per claim 5, Jacks fails to disclose: The system of Claim 1, wherein the verification event comprises one of: a read request being received, a specified clock edge occurring, and a specified number of clock edges passing. Meyer discloses a mirroring system which compares the data stored in primary and backup storage devices, and is able to correct faulty data. This can be done at clock intervals (column 6 line 60 - column 7 line 31: D flip-flop circuits synchronize at clock intervals to compare

CRC's), or when data is read incorrectly (column 5 lines 7-13). Meyer discloses this system is able to maintain consistency between two sets of mirrored data (column 1 lines 45-52) using a CRC algorithm (column 2 line 65 - column 3 line 8). Jacks also discloses that his system aims to maintain reliable backup copies of data (Jacks column 1 lines 21-33). Using Meyer's system would enable the user to maintain both data sets by periodically comparing the data at clock intervals instead of only when data is written. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the mirroring system of Meyer into the backup system of Jacks, as a means to maintain an accurate backup.

23. As per claim 11, Jacks discloses: The system of Claim 6, wherein the verification event comprises one of: a read request being received, a specified clock edge occurring, and a specified number of clock edges passing. Meyer discloses a mirroring system which compares the data stored in primary and backup storage devices, and is able to correct faulty data. This can be done at clock intervals (column 6 line 60 - column 7 line 31: D flip-flop circuits synchronize at clock intervals to compare CRC's), or when data is read incorrectly (column 5 lines 7- 13). Meyer discloses this system is able to maintain consistency between two sets of mirrored data (column 1 lines 45-52) using a CRC algorithm (column 2 line 65 - column 3 line 8). Jacks also discloses that his system aims to maintain reliable backup copies of data (Jacks column 1 lines 21-33). Using Meyer's system would enable the user to maintain both data sets by periodically comparing the data at clock intervals instead of only when data is written.

Therefore, it would have been obvious to one of ordinary skill in the art at the time Of invention to incorporate the mirroring system of Meyer into the backup system of Jacks, as a means to maintain an accurate backup.

24. As per claim 20, Jacks discloses: The method of Claim 13, wherein the verification event comprises one of: a read request being received, a specified clock edge occurring, and a specified number of clock edges passing. Meyer discloses a mirroring system which compares the data stored in primary and backup storage devices, and is able to correct faulty data. This can be done at clock intervals (column 6 line 60 - column 7 line 31: D flip-flop circuits synchronize at clock intervals to compare CRC's),. or when data is read incorrectly (column 5 lines 7-13). Meyer discloses this system is able to maintain consistency between two sets of mirrored data (column 1 lines 45-52) using a CRC algorithm (column 2 line 65 - column 3 line 8). Jacks also discloses that his system aims to maintain reliable backup copies of data (Jacks column 1 lines 21-33). Using Meyer's system would enable the user to maintain both data sets by Periodically comparing the data at clock intervals instead of only when data is written. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the mirroring system of Meyer into the backup system of Jacks, as a means to maintain an accurate backup.

Response to Arguments

25. Applicant's arguments filed 28 December 2006 have been fully considered but they are not persuasive. The Applicant argues that the prior art does not teach "original verification data for a shadow memory is calculated", "calculating current verification data for the shadow memory" and "determining whether the current verification data matches the original verification data". The Examiner respectfully disagrees.

Jacks teaches an EEPROM having data to be copied into the RAM, "shadow memory", and the EEPROM having hash sums that should reflect the state of the initialized RAM, this is interpreted as a system for verifying data in a shadow memory, comprising: a shadow memory initializer operable to detect an initialization event, to initialize a shadow memory based on the initialization event, and to calculate original verification data for the shadow memory; the shadow memory comprising a shadow data (column, 1, lines 35-61, column 4 lines 13-17, column 5 lines 7-23). Jacks also teaches checking the initializing process by generating CRC sums over the contents of the RAM and comparing them with pre-stored CRC sums, this is interpreted as a shadow memory verifier operable to detect a verification event and to verify the shadow data based on the verification event by calculating current verification data for the shadow memory and determining whether the current data matches the original verification data (column 1, lines 55-58 and column 4 lines 27-41).

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM
May 20, 2007

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100